

Digital Pulse Processor



Features

- Direct high-speed digitization of pulses from electron multipliers
- Real-time FPGA-based pulse shape analysis
- Integrated pulse-height analysis and histogram storage
- Energy discrimination not degraded at high pulse rates
- High-speed optical fiber data communication to host systems.
- Integrated HV control output, test pulser LED output and temperature sense input

Applications

- NaI scintillation detector energy spectrometry
- General electron multiplier readout

Options

- Input amplifier configuration as current to voltage or voltage to voltage converter
- Input amplifier gain selections

Specifications

Operating principle	High-speed digitization of input signal without pulse shaping amplification.
Input impedance	< 0.1 ohm in current to voltage converter configuration. Configurable option in voltage to voltage converter configuration
Input amplifier risetime	<= 50 nsec (set by anti-aliasing filtering for the ADC)
Pulse pair resolution	<= 500 nsec for pulse height analysis of both pulse <= 50 nsec for counting of both pulses
Deadtime	<= 50% pulses rejected at 500 kHz
Digitization	80 MHz 14 bit bipolar ADC with fully parallel readout to pulse processing FPGA
Pulse processing	Pulse area measurement and binning (up to 1024 channels) Pulse width discrimination Pulse overlap detection and rejection Baseline restoration



Specifications (continued)

Power input	+24 V (+/- 2 V) DC, 150 mA typical without drain on 5 V output, 200 mA max when sourcing 200 mA to 5V output.
Power output	+5 V (+/- 0.1 V) DC power output, 200 mA maximum drain.
Controls	Rotary switch for loop address
Displays	Status LEDs (power, device status, comms mode, data transmission rcv/xmit).
Case material	Stainless steel sheet.
Weight	0.27 kg (0.6 lb)
Operating environment	10 to 35 C (15 to 25 C recommended to reduce drift and offset) , < 70% humidity, non-condensing, vibration < 0.1g all axes (1 to 1000Hz)
Shipping and storage environment	-10 to 50 C, < 80% humidity, non-condensing, vibration < 2g all axes, 1 to 1000Hz

Interfacing

Interfaces	Fiber-optic loop, 10 Mbit/sec serial, 9-bit asynchronous binary. Ethernet Fiber-optic output for real time pulse data streaming to host.
Host computer	Diagnostic host program supplied for Microsoft® .net framework. DLLs available for Microsoft® .net, National Instruments™ Labview™ and Microsoft® C++.



Connectors

Signal input BNC (isolated from case)

PMT control Six pin mini-DIN female

1	HV enable out -ve	4	Analog gnd
2	HV enable out +ve	5	+5 VDC power out (200 mA max)
3	HV program out	6	Digital gnd

Test Four pin mini-DIN female

1	Test LED +ve (+5 VDC)	3	Temperature sensor (AD592 +ve)
2	Test LED -ve	4	Temperature sensor (AD592 -ve)

Fiber optics Two Avago HFBR ST bayonet for communications loop

One Avago HFBR ST bayonet for pulse data stream output

Power in 2.1mm threaded jack. Mates with Switchcraft S761K or equivalent.

Inner	+24 VDC in	Outer	0 V
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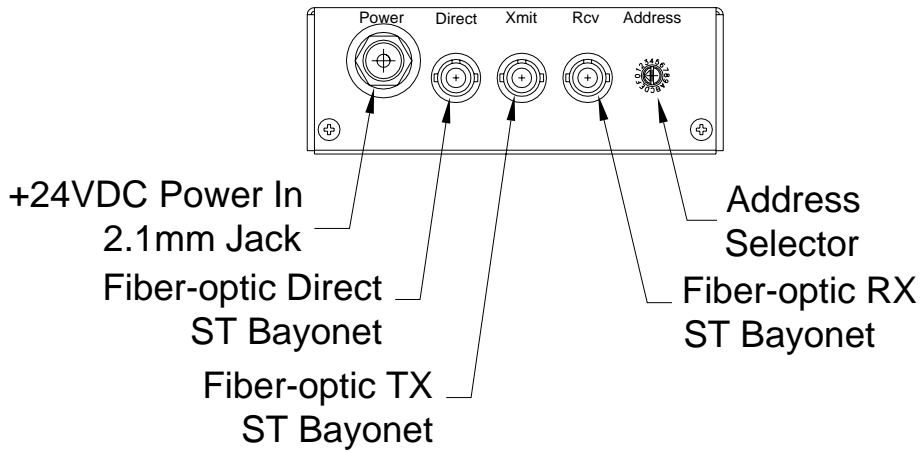
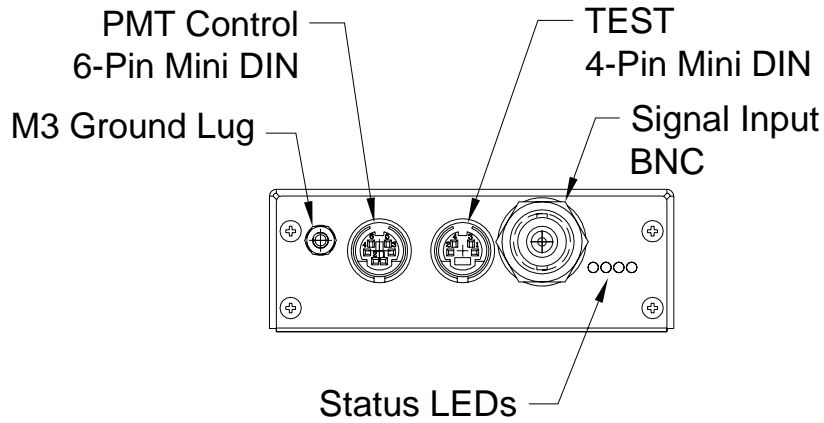
Ground M3 threaded stud

Ordering information

D100 D100 Digital Pulse Processor.

- llxx Series input impedance selection xx ohms





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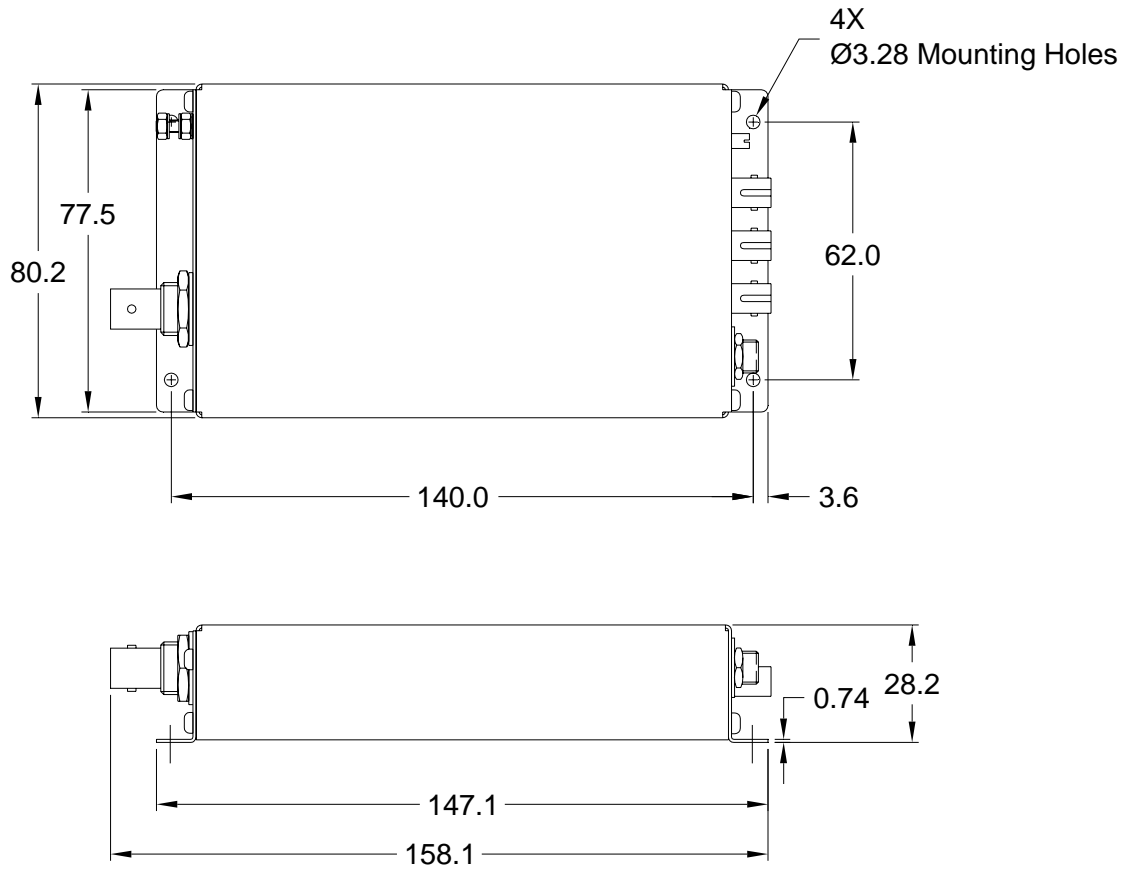
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Dims mm

